IN THE CLAIMS

Please cancel Claims 13, 23-27, 29-30 and 44-50 and Amend the remaining Claims as per the following mark-up copy:

1. (Previously Amended) A circuit for controlling a laser diode, comprising:

a bias circuit coupled to said laser diode for setting a DC operating point of said laser diode;

an amplifier having an output for superimposing an AC signal on said DC operating point, whereby said AC signal modulates an intensity of light emitted by said laser diode, and wherein said amplifier has a control input for controlling a maximum output swing of said amplifier;

at least one capacitor connected in functional series between said output of said amplifier and a terminal of said laser diode, whereby said AC signal is capacitively coupled to said laser diode;

a control circuit coupled to said control input of said amplifier for setting said maximum output swing of said amplifier; and

a programmable memory coupled to said control circuit for storing values for controlling said maximum output swing, whereby an amplitude of said AC signal is controlled, thereby controlling

said modulation independently from settings of said DC operating point.

2. (Original) The circuit of Claim 1, wherein said programmable memory is a one-time-programmable memory.

3. (Original) The circuit of Claim 1, wherein said programmable memory is an electrically-erasable memory.

4. (Original) The circuit of Claim 1, wherein said control circuit comprises a current source coupled to said programmable memory and having an output coupled to said control input of said amplifier for providing control of said maximum output swing in response to settings within said programmable memory.

5. (Original) The circuit of Claim 4, wherein said programmable memory is a analog memory, and wherein said current source comprises a voltage controlled current source having an input coupled to an output of said analog memory and an output coupled to said amplifier for controlling said maximum output swing.

6. (Original) The circuit of Claim 4, wherein said current source comprises a digitally programmable current source.

7. (Original) The circuit of Claim 6, wherein said digitally programmable current source comprises:

a plurality of current sources having a fixed current scaled in sequence by powers of two; and

a plurality of switches, wherein each of said plurality of switches is coupled to an associated one of said plurality of current sources, whereby a digital signal set coupled to control inputs of said plurality of switches sets a current level determined by a binary value of said digital signal set.

8. (Original) The circuit of Claim 7, wherein said digitally programmable current source further comprises a shift register having a plurality of bit storage latches, wherein each of said plurality of latches is coupled to an associated one of said plurality of switches, whereby data from said programmable memory may be shifted in to control said plurality of switches to set said current level.

9. (Previously Amended) A circuit for controlling a laser diode, comprising:

a bias circuit coupled to said laser diode for setting a DC operating point of said laser diode;

a modulation signal source having an output for superimposing an AC signal on said DC operating point, thereby modulating an intensity of light emitted from said laser diode;

at least one capacitor connected in functional series between said output of said modulation source and a terminal of said laser diode, whereby said AC signal is capacitively coupled to said laser diode;

a programmable memory for storing values for controlling parameters of said circuit; and

means for controlling a maximum swing of said modulation signal source independently from settings of said DC operating point in conformity with said stored values.

10. (Previously Amended) A method for operating a laser diode, comprising:

retrieving values stored in a programmable memory;

biasing said laser diode at a DC operating point;

modulating an intensity of said laser diode with a modulating signal from an amplifier, by passing said modulating signal through at least one capacitor connected in functional series between an output of said amplifier and a terminal of said laser diode; and

controlling a an amplitude of said modulating signal by controlling a maximum swing of said amplifier in conformity with said retrieved values.

11. (Original) The method of Claim 9, wherein said modulating is performed via an amplifier having settable maximum and minimum output levels, and wherein said controlling sets said maximum and minimum output levels.

12. (Currently Amended) A circuit for controlling a laser diode, comprising:

a bias circuit coupled to said laser diode for setting a DC operating point of said laser diode;

an amplifier having an output coupled to said laser diode for superimposing an AC signal on said DC operating point;

a programmable memory for storing values for controlling a transition time of said AC signal; and

a control circuit for coupling said output of said amplifier to said laser diode, said control circuit having an adjustable response whereby ~~a~~ said transition time of said AC signal may be adjusted, and wherein said control circuit is further coupled to said programmable memory for adjusting said transition time in conformity with said values stored in said programmable memory, and wherein said control circuit is a capacitor array having a

selectable capacitance for setting a coupling capacitance coupling said output of said amplifier to said laser diode, whereby said transition time is set in conformity with said selectable capacitance.

13. Canceled

14. (Currently Amended) The circuit of Claim 12[[3]], wherein said capacitor array comprises:

a plurality of capacitors having a capacitance scaled in sequence by powers of two; and

a plurality of switches, wherein each of said plurality of switches is coupled to an associated one of said plurality of capacitors, whereby a digital signal set coupled to control inputs of said plurality of switches sets a capacitance determined by a binary value of said digital signal set.

15. (Previously Amended) The circuit of Claim 14, wherein said capacitor array further comprises a shift register having a plurality of bit storage latches, wherein each of said plurality of latches is coupled to an associated one of said plurality of switches, whereby data from said programmable memory may be shifted in to control said plurality of switches to set said capacitance.

Claims 16-17 were previously canceled.

18. (Original) The circuit of Claim 12, wherein said amplifier has a control input for controlling maximum output swing of said amplifier, and wherein said programmable memory is further coupled to said control input for setting said maximum output swing.

19. (Original) The circuit of Claim 18, further comprising a second control circuit coupled to said programmable memory and having an output coupled to said control input of said amplifier for providing control of said maximum output swing in response to settings within said programmable memory.

20. (Previously Amended) The circuit of Claim 19, wherein said second control circuit comprises a programmable current source having an input for receiving at least one signal corresponding to said settings supplied from said programmable memory, whereby an output of said programmable current source provides a current level responsive to a value of said settings.

21. (Original) The circuit of Claim 20, wherein said programmable current source comprises:

a plurality of current sources having a fixed current scaled in sequence by powers of two; and

a plurality of switches, wherein each of said plurality of switches is coupled to an associated one of said plurality of current sources, whereby a digital signal set coupled to control inputs of said plurality of switches sets a current level determined by a binary value of said digital signal set.

22. (Original) The circuit of Claim 21, further comprising a shift register having a plurality of bit storage latches, wherein each of said plurality of latches is coupled to an associated one of said plurality of switches, whereby data from said programmable memory may be shifted in to control said plurality of switches to set said current level.

Claims 23-27 have been canceled.

28. (Previously Amended) An integrated circuit for controlling a laser diode, wherein said integrated circuit comprises:

a bias control circuit for controlling a DC operating point of said laser diode;

a swing control circuit for controlling the maximum amplitude of an AC modulating signal via controlling the maximum swing of an external amplifier via an external terminal of said

amplifier provided for controlling said external amplifier, whereby an output said amplifier when connected via an external at least one capacitor in functional series to a terminal of said laser diode superimposes an amplitude-controlled signal version of said AC modulating signal having an amplitude responsive to said swing control circuit; and

a programmable memory for supplying programmed values to said bias control circuit and said swing control circuit whereby said maximum amplitude and said DC operating point are independently set in conformity with said programmed values.

Claims 29-30 are Canceled.

31. (Currently Amended) An integrated circuit for controlling a laser diode, wherein said integrated circuit comprises:

a bias control circuit for controlling a DC operating point of said laser diode;

a response control circuit for controlling the transition time of an AC modulating signal coupled to said laser diode;

a programmable memory for supplying programmed values to said bias control circuit and said response control circuit whereby said transition time and said DC operating point are set in conformity with said programmed values; and a swing control circuit for controlling a maximum swing of said AC modulating

signal, and wherein said programmable memory is further used for supplying programmed values to said swing control circuit whereby said maximum swing of said modulating signal and said DC operating point are set in conformity with said programmed values; and ~~The integrated circuit of Claim 30, further comprising~~

an under-voltage lockout circuit for preventing operation of said bias control circuit unless a voltage supplied to said integrated circuit exceeds a predetermined level.

32. (Currently Amended) The integrated circuit of Claim 31[[0]], wherein said bias control circuit comprises a bandgap reference for supplying a reference voltage for generating a laser bias voltage, and wherein said undervoltage lockout circuit disconnects an output of said bandgap reference unless a voltage from said bias control circuit exceeds a predetermined level.

33. (Currently Amended) The integrated circuit of Claim 31[[0]], further comprising a power on reset circuit for preventing operation of said bias control circuit until an initialization time has elapsed.

34. (Original) The integrated circuit of Claim 33, wherein said bias control circuit comprises a bandgap reference for supplying

a reference voltage for generating a laser bias voltage, and wherein said power on reset circuit disconnects an output of said bandgap reference from said bias control circuit until said initialization time has elapsed.

35. (Currently Amended) The integrated circuit of Claim 34, ~~further comprising an under-voltage lockout circuit for preventing operation of said bias control circuit until a voltage supplied to said integrated circuit has reached a predetermined level, and~~ wherein a start of said initialization time is determined by the end of said under-voltage lockout circuit preventing operation.

36. (Original) The integrated circuit of Claim 35, further comprising:

a logic AND gate for combining said output of said power on reset circuit and an output of said under-voltage lockout circuit; and

a buffer for coupling said output of said bandgap reference to said bias control circuit, said buffer having a control input for disabling said buffer, wherein said control input is coupled to an output of said logic AND gate for disconnecting said bias control circuit until a voltage supplied to said integrated

circuit has reached a predetermined level and until said initialization time has elapsed.

37. (Currently Amended) A circuit for controlling a laser diode, comprising:

a bias circuit coupled to said laser diode for setting a DC operating point of said laser diode, said bias circuit having a power supply input coupled to a power supply rail;

a voltage reference coupled to said power supply rail for biasing a monitor diode optically coupled to said laser diode, such that variations in said power supply rail are not reflected in the bias imposed on said monitor diode, and wherein said voltage reference is further coupled to said bias circuit; and

a programmable memory coupled to said bias circuit for setting said DC operating point; and

an under-voltage lockout circuit;

a power-on reset circuit, wherein said under-voltage lockout circuit and said power-on reset circuit are coupled to said voltage reference for disabling said voltage reference until a voltage supplied to said integrated circuit has reached a predetermined level and an initialization time has elapsed.

38. (Original) The circuit of Claim 37, wherein said programmable memory is a one-time-programmable memory.

39. (Original) The circuit of Claim 37, wherein said programmable memory is an electrically erasable memory.

40. (Currently Amended) The circuit of Claim 37, ~~wherein~~ further comprising a bias resistor for coupling an output of said voltage reference to said monitor diode, whereby a gain of said bias circuit can be set by the value of said bias resistor.

41. (Previously Amended) The circuit of Claim 37, wherein said bias circuit includes a resistor array having a selectable resistance value, wherein said resistance value is selected via values stored within said programmable memory.

42. (Original) The circuit of Claim 37, wherein said programmable memory is an analog memory and wherein said bias circuit further comprises a transistor having a gate coupled to an output of said analog memory for producing a resistance for controlling said bias circuit in conformity with values stored within said analog memory.

43. (Original) The circuit of Claim 42, wherein said bias circuit further comprises a voltage controlled current source coupled to said monitor diode including a resistor having thermal resistance variation characteristics matched to thermal resistance variation characteristics of said programmable resistor array, whereby thermal variations in said resistor and said resistor array are cancelled.

Claims 44-50 are Canceled.